Verification Design student

Location: Yokneam and Petach Tikva

Description:

We are offering you a great opportunity to join the Switch IP department and be part of the IP development for the next generation Switch.

As a student in the IP department you’ll be responsible for design and verification of ASIC/VLSI of a complex IP.

You will be working with Verilog, System Verilog, UVM, C++, Perl, Python, System C

You will become a design and verification engineer.

Qualifications:

- Student for Electrical engineering B.Sc
- Knowledge of logical gates
- Knowledge in programming
- Good learning skills
- Problems solving skill
- Ability to be a part of a team, working in cooperation