Formal Verification student - Petah Tikva

We are offering you a great opportunity to join the Formal Verification team at the Switch IP department and be a part of the IP development for the next generation Switch.

As a student in the Formal Verification team you’ll be responsible for the verification of ASIC/VLSI of a complex IP and for the development of complex Formal Verification structures.

You will be working with Verilog, System Verilog, SVA, Perl, Python

You will become an expert verification and formal engineer.

Qualifications:

- Student for Electrical engineering B.Sc
- Knowledge of logical gates
- Knowledge in programming
- Good learning skills
- Problems solving skill
- Ability to be a part of a team, working in cooperation