**Senior VLSI Designer**

**Responsibilities:**

- Handling RTL design for new blocks and legacy blocks, chip integration, block level and top level verification, RTL simulations and gate level simulations.
- Close work with architecture and system groups for design specification definitions and implementation impacts.
- Block level synth, lint, integrating and supporting DFT structures.
- Support BE team during chip implementation for design related topics as well as production and validation teams tests ramp up.

Bachelor's degree in Electrical Engineering or Computer Engineering from a leading university.

- Min 4 years’ experience as VLSI front-end engineer.
- Experience with Verilog and System Verilog design coding. (VHDL design is a plus)
- Experience with block level verification and full chip verification. (SV verification is a plus)
- Experience in gate level debug
- Experience with legacy code understanding, debugging and problems solving attitude
- Familiar with unix/linux and scripting languages (perl / TCL/ csh)
- Experience with AMBA/AXI - an advantage
- Experience with Cadence tools flow - an advantage
- Experience with Synthesis and STA analysis - an advantage
- Good communication skills
- Innovator, brings out of the box solutions
- Team player

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