Transaction base model in SystemC(C++)

November 2016
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• Research Title: Transaction base model in SystemC(C++)

• Project Schedule
  – Two semesters

• Suggested format: Undergraduate project

• Site: PTK
transaction base model in SystemC

Background:

• Writing models for RTL in C++ has several advantages:
  – Can be used as golden model
  – Can be used for architecture research (modeling)
  – C++ is a known language
  – Very fast (compilation & simulation)
  – SystemC contains a reach simulation kernel to enable designers write good test benches easily (for example data types used in Verilog)

• Current C++ solution (Verifier) is limited (not as reach as SystemC)

Goals of this project:

– Create SystemC model for one of the units
– Integrating model with current test benches (UVM, coverage)
– Helping with methodology definition for SystemC modeling
Academic Prerequisite Requirements

• Background in C/C++ programing
• Background in verilog/VHDL languages - advantage
SystemC model integrated in UVM env