Networking packet processor creation

November 2016
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• Research Title: Build a networking processor CPU

• Project Schedule
  – Two semesters

• Suggested format: Undergraduate project

• Site: PTK
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Background:

• In modern switches, programmability and flexibility is a required feature
• General purpose CPU cannot handle the very high packet rate
• Custom CPU + ASIC can be both flexible and handle high rates
  – However, it has high development effort
  – The CPU compiler is not aware of the surrounding ASIC

Goals of this project:

– Define CPU extensions using Tensilica core TIE language
– Build the custom CPU using Tensilica compiler
– Run programs on the Tensilica simulator
– Synthesize and compare to existing CPU+ASIC solution
Academic Prerequisite Requirements

- Background in C programming
- Background in verilog/VHDL languages
Tensilica CPU development flow

1. Select from menu
2. Explicit instruction description (TIE)

Xtensa Processor Generator*

Complete Hardware Design
Pre-verified RTL
EDA scripts
test suite

Processor Extensions
Use standard ASIC/COT design techniques and libraries for any IC fabrication process

Customized Software Tools
C/C++ compiler
Debuggers
Simulators
RTOSes

Iterate in Minutes!