Automatic Registers Generator
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• Research title:
  Build an optimized automatic registers generator

• Project Schedule
  – Two semesters by one student

• Suggested format:
  Undergraduate project

• Site: PTK
Automatic Registers Generator

Background:
- Switch devices are using many registers in the design
- The registers are well described by a database
- Any automatic process in ASIC-designs can reduce effort dramatically
- Many backend optimizations can be done on registers in order to reduce power/area/timing of the devise

Goals:
- Study Marvell’s registers architecture
- Learn the registers database
- Look for RTL optimizations in the registers design
- Describe the optimization method
- Implement the method on the registers automated tool
Project Requirements

• High motivation
• Ability to learn complex systems
• Team-work
• Flexible working hours

Academic Requirements

• Background in the VLSI/Chip-Design industry (design & backend)
• Background in Programing
Registers Automatic Flow