UVM Packet Generator
UVM Packet Generator

• Research title:
  Build a generic UVM Packet Generator

• Project Schedule
  – Two semesters by two students

• Suggested format:
  Undergraduate project

• Site: PTK
UVM Packet Generator

Background:
• Switch Device main idea is to deliver a data-packet from one place to another.
• UVM is a high-level language commonly used by the industry, that used to build verification environments for VLSI devices.

Goals:
• Study industry’s usage of packet generators
• Study networking protocols
• Learn UVM
• Plan desired implementation
• Building a UVM packet generator that will be used to verify one of Marvell’s devices
Project Requirements

• High motivation
• Ability to learn complex systems
• Team-work
• Flexible working hours

Academic Requirements

• Background in the VLSI/Chip-Design industry (design & verification)
• A Preview for Networking
• Background in Object oriented Programing
Packet generator